REMARKS

Rejections

Claims 1-17 are presently pending. Claims 1-17 stand rejected. Claim 18 is added. Claims 1-4, 8-12, and 16-17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Linzer. Claims 5 and 13 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Ju. Claims 6, 7, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Lavelle.

Comments directed to all claims

As an initial matter, Assignee has reviewed the Examiner's application of Linzer in response to the Assignee's remarks in the previous response. Assignee continues to believe that Linzer does not disclose that the exact same data is duplicated at two different addresses in the memory. The Examiner cited pg. 4, [0040], lines 1-6 of Linzer as disclosing "storing the data in the machine readable memory device a second time at a second memory address" of Assignee's claims.

The cited excerpt of Linzer at pg. 4, [0040] (including lines 1-6) reads as follows:

> **[0040]** A 2-cycle burst generally provides a 2×8 region from one field (e.g., 2-byte aligned vertically, 8-byte aligned horizontally). In two such bursts, a 2×16 region from one field (e.g., 2-byte aligned vertically, 8-byte aligned horizontally) may be obtained that may cover any 9 pixels horizontally. At most 6, but on average 5.5, 2×16 field regions may cover a 9×9 pixel region -in the frame, as may be summarized in the following TABLE 2. The total number of cycles taken to retrieve the 9×9 region may be expressed by 2*2*6=24 cycles in a worst case scenario and 22 for an average case scenario.

Assignee submits that there is no disclosure in Linzer paragraph [0040] of "storing the data in the machine readable memory device a second time at a second memory address" of Assignee's claims.

Nevertheless, Assignee has amended its claims to more clearly define the invention and has added to all of the independent claims - claims 1, 9, 16 and 17 - the limitation that "the second alignment [is] offset from the first alignment relative to the burst boundaries, the offset sufficient to enable selection for retrieval of the data from the first alignment or second alignment."

Assignee submits that none of the cited references disclose that "the second alignment [is] offset from the first alignment relative to the burst boundaries, the offset sufficient to enable selection for retrieval of the data from the first alignment or second alignment."

Accordingly, for this reason, alone, Assignee respectfully traverses the rejection to all of the

independent claims 1, 9, 16, and 17, and dependent claims 2-8 and 10-15 and requests that Examiner withdraw it. New claim 18 is allowable for the same reasons.

Assignee further continues to believe that the arguments set forth in its previous response distinguish its claimed invention from the cited references, especially in light of the amendments to the independent claims. The following remarks reiterate the remarks of Assignee's previous response and are equally applicable to the claims as currently amended.

Comments directed to claim 1, and dependent claims 2-8

Claim 1 recites, "the first memory address having a first alignment with respect to the burst boundaries; ... the second memory address having a second alignment with respect to the burst boundaries." Examiner has indicated that Linzer teaches "a first alignment with respect to the burst boundaries (pg. 4, [0033], lines 12-14); ... the second address having a second alignment with respect to the burst boundaries" (pg. 4, [0040], lines 1-6).

Lines 12-14 of Linzer, [0033], appear on pg. 3 (not pg. 4) and Assignee assumes that the Examiner is referencing lines 12-14 of [0033] on pg. 3. Linzer, pg. 3-4, [0033], lines 11-17 (which include lines 12-14) recite that "When the memory 102 is implemented as one 32-bit wide chip, a burst may comprise 16 bytes aligned to a 16 byte boundary. When the memory 102 is implemented with two 16-bit wide chips (e.g., the memories 142 and 144 may be

implemented with 16-bit wide memory chips), a burst may comprise 8 bytes aligned to an 8 byte boundary from each of the memory chips."

Linzer, pg. 4, [0040], lines 1-6 recites "A 2-cycle burst generally provides a 2x8 region from one field (e.g., 2 byte aligned vertically, 8 byte aligned horizontally). In two such bursts, a 2x16 region from one field (e.g., 2-byte aligned vertically, 8-byte aligned horizontally) may be obtained that may cover any 9 pixels horizontally."

It is respectfully submitted that the foregoing does not teach "the second memory address having a second alignment with respect to the burst boundaries". As discussed generally, above in connection will all claims, the foregoing does not even teach "a second address", nor its particular "alignment with respect to the burst boundaries", much less "storing the data in the machine readable memory device a second time at a second memory address, the second memory address having a second alignment with respect to the burst boundaries". Accordingly, for the foregoing reason, Assignee respectfully traverse the rejection to claim 1, and dependent claims 2-8 and requests that Examiner withdraw it.

Comments directed to claim 9, and dependent claims 10-15

Claim 9 recites, "retrieving the desired bytes of data from a preferred memory address, the preferred memory address being aligned with the at least one burst boundary

such that the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses". Examiner indicates that the foregoing limitation is described at Linzer, p. 8, [0061], lines 1-10. Linzer [0061], merely describes "an example access pattern for a line mode in accordance with the present invention." Linzer, [0061], lines 1-3. The foregoing has no teaching that "the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses". Accordingly, for at least this reason as well, Assignee respectfully traverses the rejection of claim 9, and dependent claims 10-15 and requests that Examiner withdraw it.

Comments directed to claim 16

Claim 16 recites, "a circuit for writing the data to the machine readable memory device a first time starting at the first memory address that has the first alignment with respect to the burst boundaries and writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries".

Examiner has indicated that Linzer teaches this element at abstract lines 2-8 and pgs. 3-4, [0033], lines 11-17. Abstract lines 2-8 disclose storing "one first pixel from a first field of a frame of the image" and separately storing "a second pixel from a second field of

the frame of the image." Abstract lines 2-8 do not disclose storing the same data twice at two different addresses as in Assignee's claims. The same is true for Linzer, pgs. 3-4, [0033], lines 11-17. Linzer, pg. 3-4, [0033] does not disclose storing data at two different addresses. Instead, this excerpt of Linzer discloses two alternative chip implementations not to be used concurrently but one in place of the other. Linzer, [0033] does not disclose storing the same data twice at different memory addresses.

Comments directed to claim 17

Claim 17 recites, among other limitations, a machine readable memory device "for storing data starting at a first memory address that has a first alignment with respect to burst boundaries, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries". Examiner has cited Linzer, pg. 3, [0033], lines 11-14, and Linzer pg. 3-4, [0033], lines 11-17 as disclosing, respectively, the data stored at a first memory address and data stored at a second memory address. Linzer, pg. 3-4, [0033] does not disclose storing data at two different addresses. Instead, this excerpt of Linzer discloses two alternative chip implementations not to be used concurrently but one in place of the other. Linzer, [0033] does not disclose storing the same data twice at different memory addresses.

Additionally, claim 17 recites, among other limitations, "a circuit for determining a first number of bursts for retrieving the data from the first address and

determining a second number of bursts for retrieving the data from the second address and retrieving the data from the first address if the first number of bursts is fewer than the second number, and retrieving the data from the second address if the second number of bursts is fewer than the first number".

Examiner has cited Linzer pg. 2, [0020], lines 2-6, fig 5B, pg. 2 [0022]-[0023], and pg. 3, [0032], lines 1-6 as disclosing this element. Those excerpts of Linzer, however, only discuss the memory configuration of Linzer and "which one of the address bits of the memories 142 and 144 is controlled by the signals ADDR_L and ADDR_R". These excerpts of Linzer do not disclose comparing the number of bursts necessary for retrieving identical data from two different addresses and then retrieving the data from the address requiring fewer bursts, as Assignee claims.

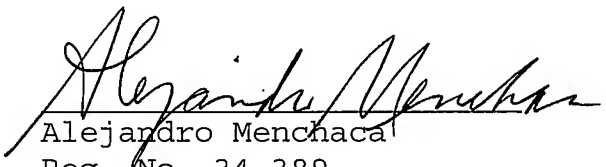
Accordingly, for at least this additional reason, Assignee submits that claim 17 is allowable.

Conclusion

For at least the foregoing reasons, Assignee respectfully submits that the application is in a condition for allowance and a notice of allowance is respectfully requested.

The Commissioner is hereby authorized to charge any fees in connection with any of the actions requested herein to deposit account number 13-0017.

RESPECTFULLY SUBMITTED



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